AMENDMENT TO THE SPECIFICATION

Please replace the paragraph beginning on page 2, line 26 and ending on page 3, line 20 (i.e., paragraph [0008] of the instant published application No. 2002/0101985) of the instant specification with the following amended paragraph:

In one implementation of the invention, the Data Encryption Standard (DES) algorithm is implemented in combinational logic which performs the encryption or decryption in one hardware cycle. The DES algorithm, as set forth in Federal Information Processing Standards Publication FIPS PUB [[463]] 46-3, ~~as reaffirmed Oct. 25, 1999,~~ from the National Institute of Standards and Technology of the U.S. Department of Commerce, is designed to encipher and decipher blocks of data consisting of 64 bits under control of a 64-bit key. A block to be enciphered is subjected to an initial permutation and then to a complex key-dependent computation and finally a permutation which is the inverse of the initial permutation. Deciphering is accomplished by using the same key as for enciphering, but with a schedule of addressing the key bits altered so that the deciphering process is the inverse of the enciphering process. The computation which uses the permuted input block as its input to produce the pre-output block consists, but for a final interchange of blocks, of sixteen iterations of a calculation which operates on two blocks, one of 32 bits and one of 48 bits, and produces a block of 32 bits. In prior hardware implementations, registers are required to store the intermediate results of these sixteen iterations requiring sixteen clock cycles to accomplish the computations, but the combinatorial logic used to implement the algorithm according to the teachings of the present invention perform the computations in one hardware cycle that is approximately ten clock cycles.

Please replace the "Brief Description of the Drawings" section of the instant specification with the following amended section:

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

~~Figure 1 is~~ Figs. 1A and 1B show a logic diagram of a hardware implementation of the DES encryption algorithm; and

~~Figure 2 is~~ Figs. 2A and 2B show a logic diagram of a hardware implementation of the DES decryption algorithm.